

MC14008B

4-Bit Full Adder

The MC14008B 4-bit full adder is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

Features

- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B
- These Devices are Pb-Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

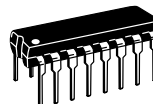
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



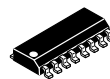
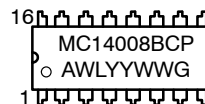
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MARKING DIAGRAMS



PDIP-16
P SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



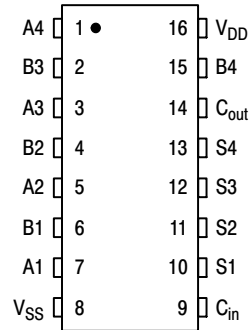
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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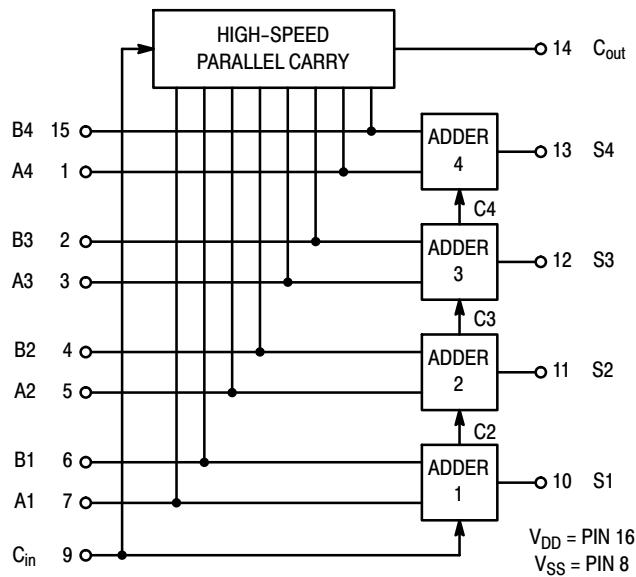
PIN ASSIGNMENT



TRUTH TABLE (One Stage)

C _{in}	B	A	C _{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]
MC14008BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14008BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
15		—	0.05	—	0	0.05	—	0.05	—	
V _{in} = 0 or V _{DD}	"1" Level V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
15		—	4.0	—	6.75	4.0	—	4.0	—	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"1" Level V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—	
10		- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
15		- 4.2	—	- 3.4	- 8.8	—	- 2.4	—		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (1.7 μA/kHz) f + I _{DD} I _T = (3.4 μA/kHz) f + I _{DD} I _T = (5.0 μA/kHz) f + I _{DD}							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

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SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Sum in to Sum Out t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 127 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$ Sum In to Carry Out t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 220 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 112 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$ Carry In to Sum Out t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 290 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$ Carry In to Carry Out t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 85 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	400 160 115 305 145 110 375 155 115 170 75 55	800 320 230 610 290 220 750 310 230 340 150 110	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

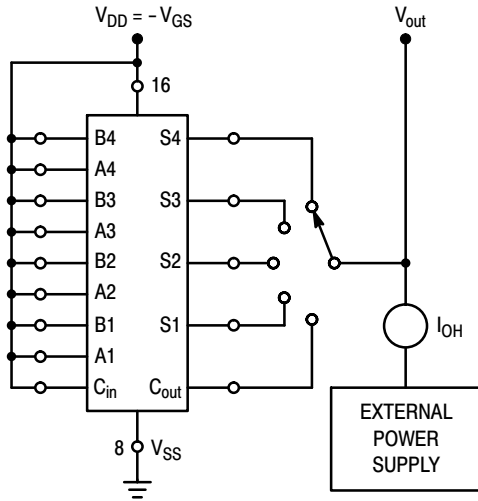


Figure 1. Typical Source Current Characteristics Test Circuit

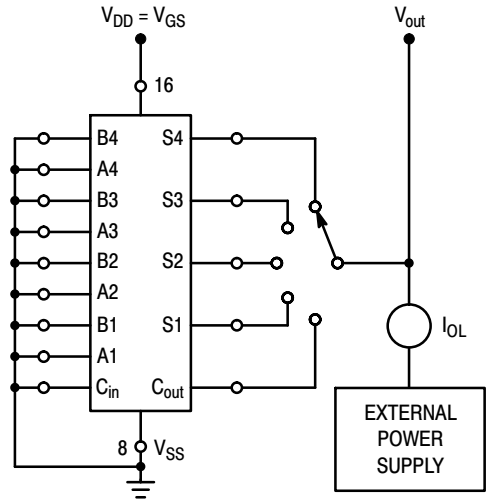


Figure 2. Typical Sink Current Characteristics Test Circuit

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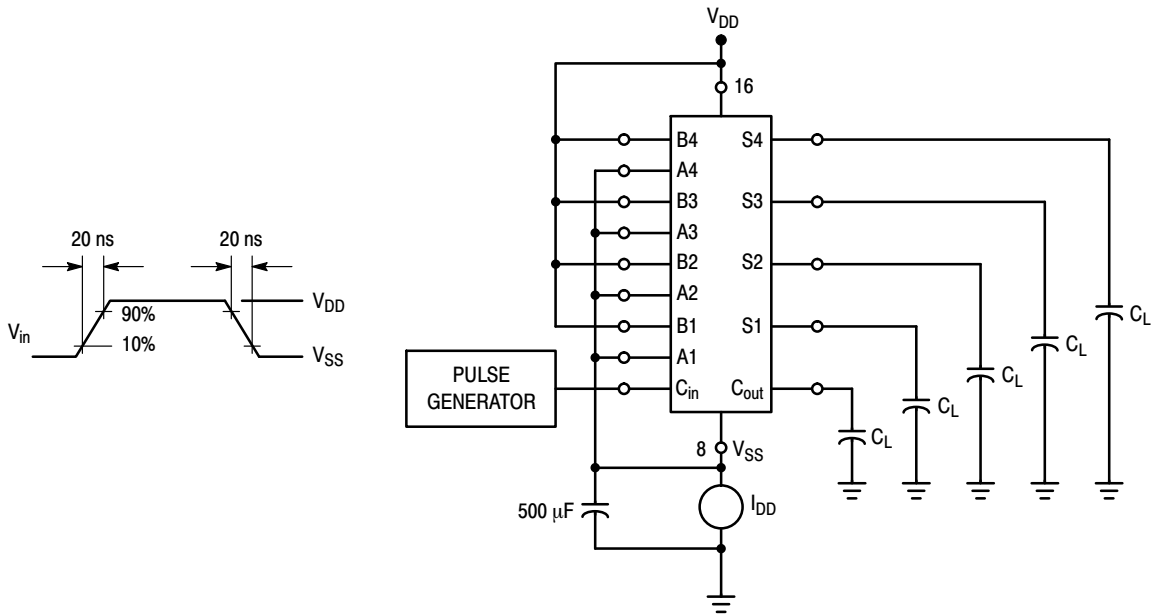


Figure 3. Dynamic Power Dissipation Test Circuit and Waveform

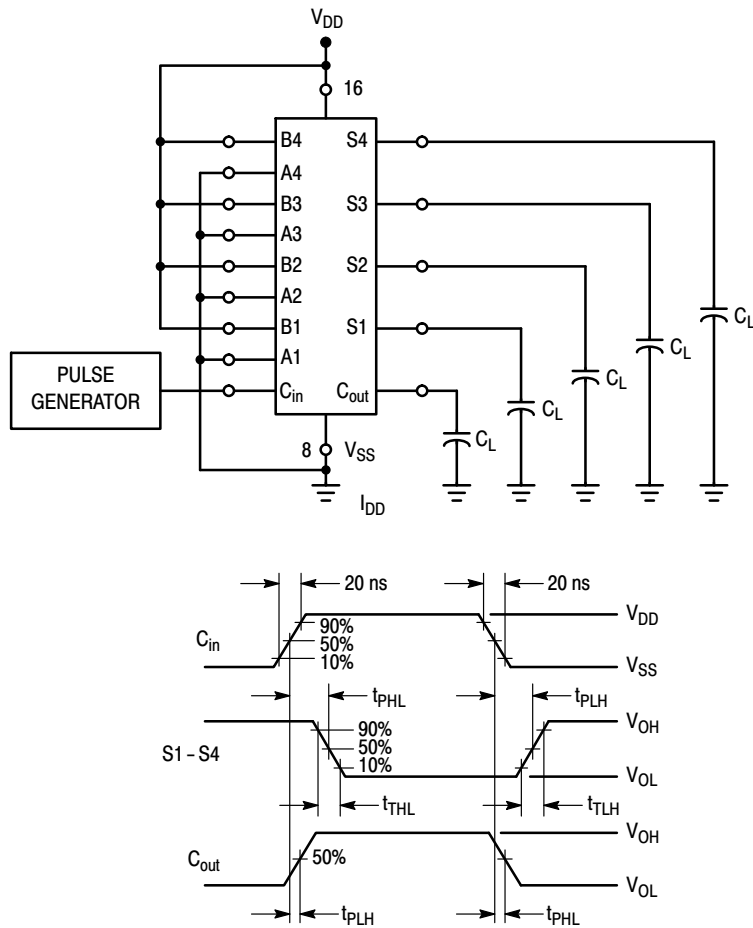


Figure 4. Switching Time Test Circuit and Waveforms

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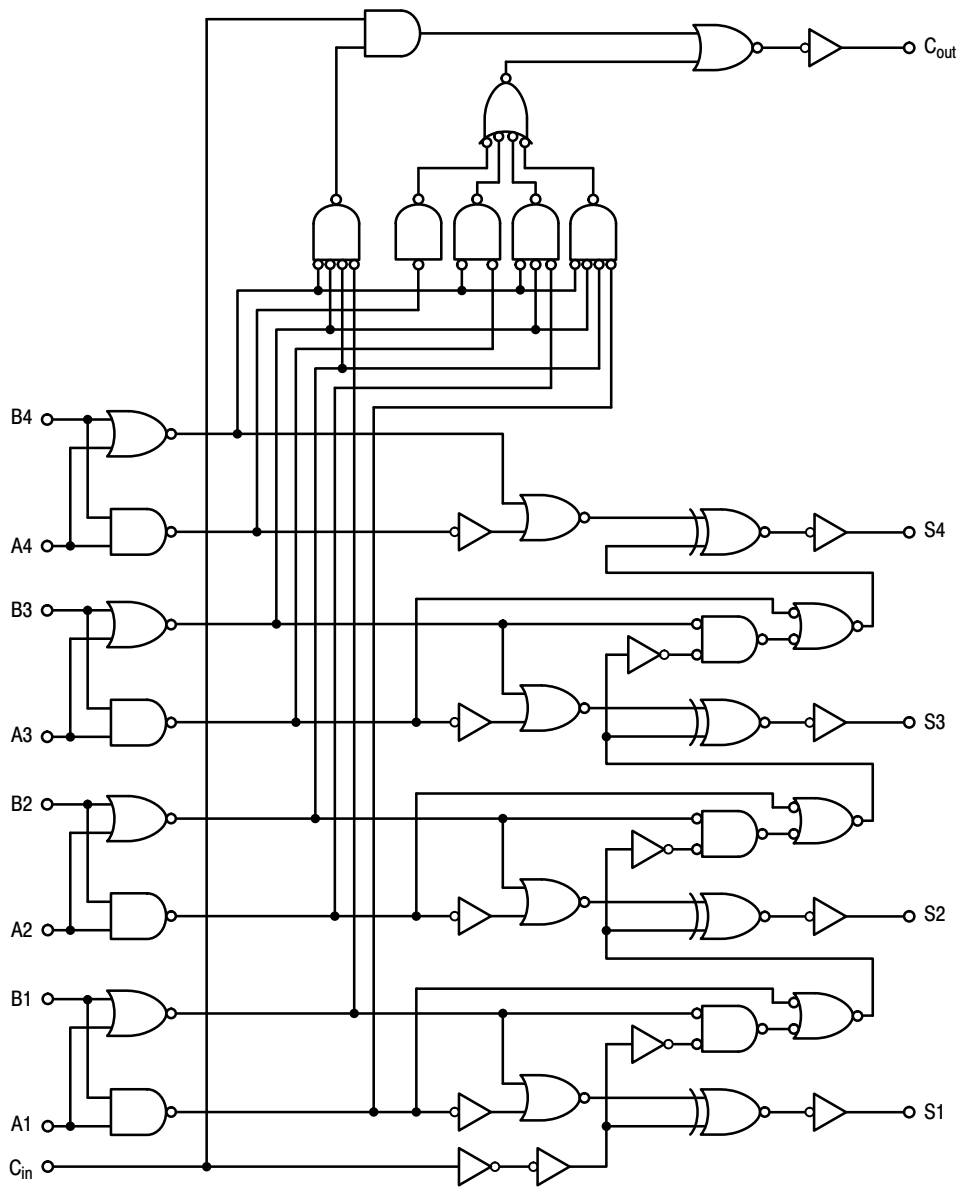
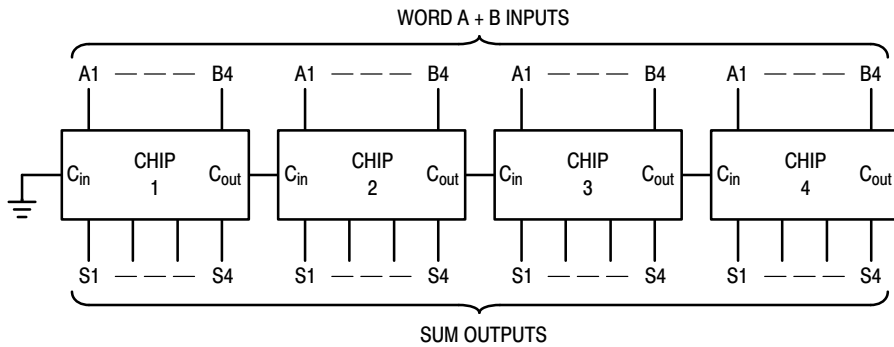


Figure 5. Logic Diagram

TYPICAL APPLICATION



Calculation of 16-bit adder speed:

$$t_p \text{ total} = t_p (\text{Sum to Carry}) + t_p (\text{Carry to Sum}) + 2 t_p (\text{Carry to Carry})$$

The guaranteed 16-bit adder speed at 10 V, 25°C, $C_L = 50 \text{ pF}$ is:

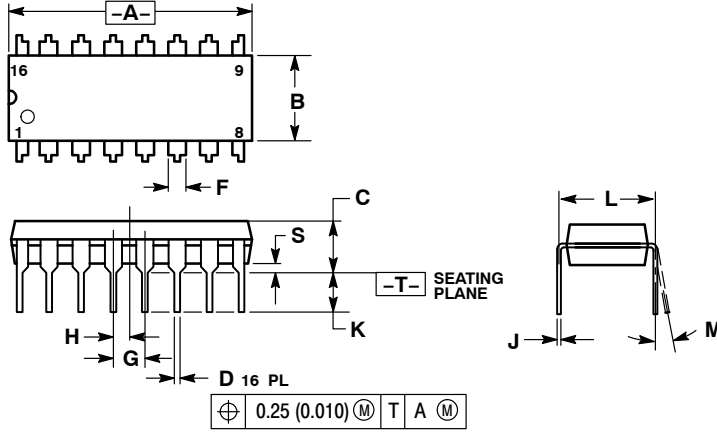
$$t_p \text{ total} = 290 + 310 + 300 = 900 \text{ ns}$$

Figure 6. Using the MC14008B in a 16-Bit Adder Configuration

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PACKAGE DIMENSIONS

PDIP-16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648-08
ISSUE T



NOTES:

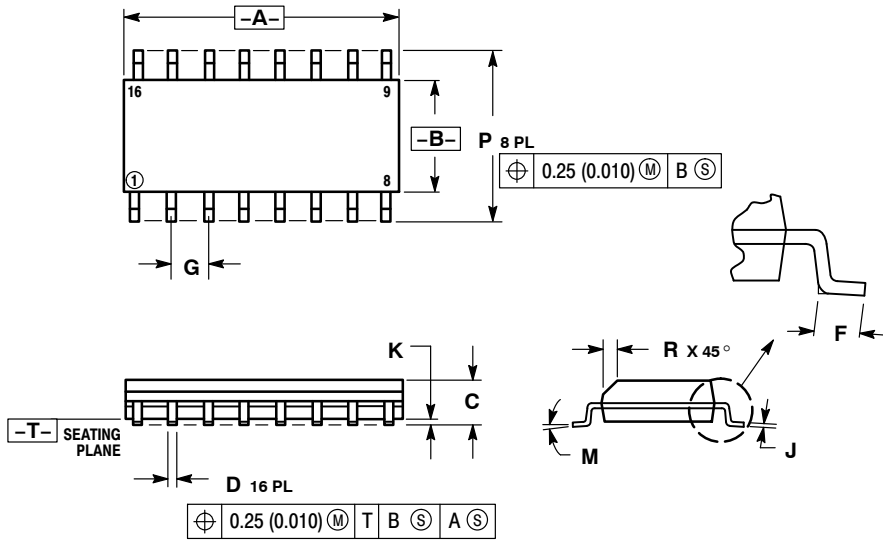
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

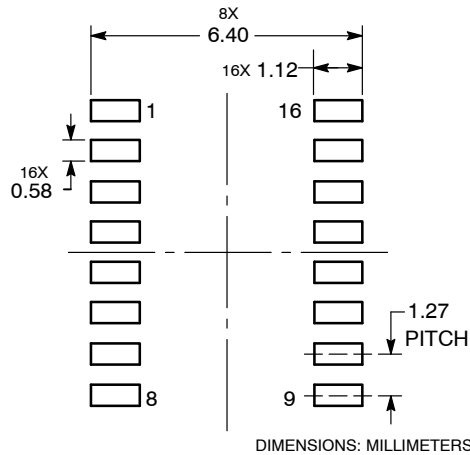


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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